FACULTY OF SCIENCE

FINAL EXAMINATION

PHYSICS 328
Electronics

Examiner: Sidney Gulick December 13, 2004

Associate Examiner: Prof. John Crawford 14:00-17:00

INSTRUCTIONS: Answer all questions. All questions have equal weight

Answers are to be given in the examination booklets.

No notes or books are to be permitted.

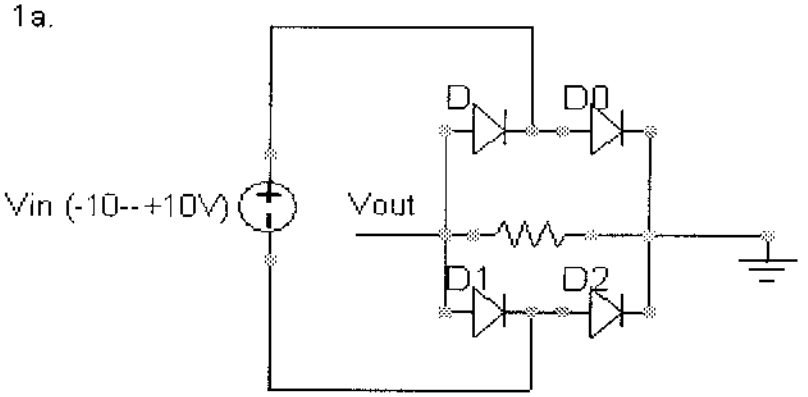
Calculators may be used.

This exam comprises 6 questions and 7 pages.

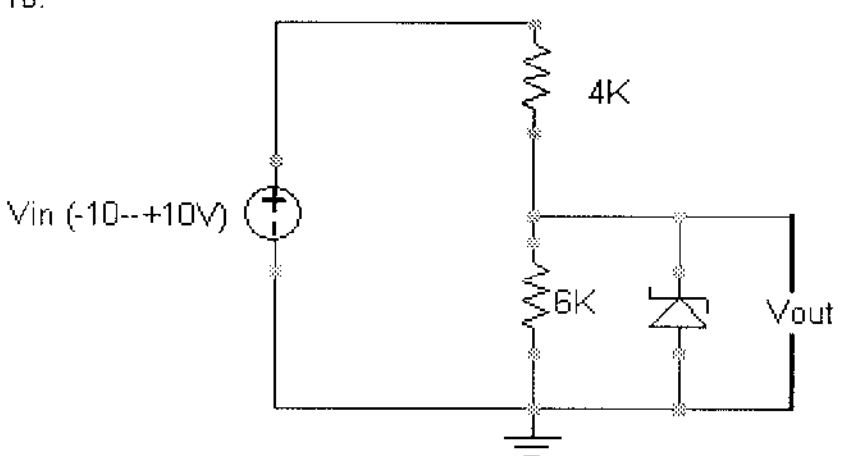
Feel free to make approximations which preserve the essential characteristics of the circuits to be analyzed but acknowledge that you have made them.

1. Consider circuits 1a and 1b. For each circuit, plot Vout (y) vs. Vin (x) for a linear ramp voltage Vin which goes from -10V to +10V. Indicate any kinks or discontinuities in the graphs. Consider the diodes to have 0 internal resistance and to conduct with a forward bias of .6V. Consider the Zener diode to act like an ordinary diode when forward biased and when reverse biased until its breakdown voltage of 5V is reached.

1a.



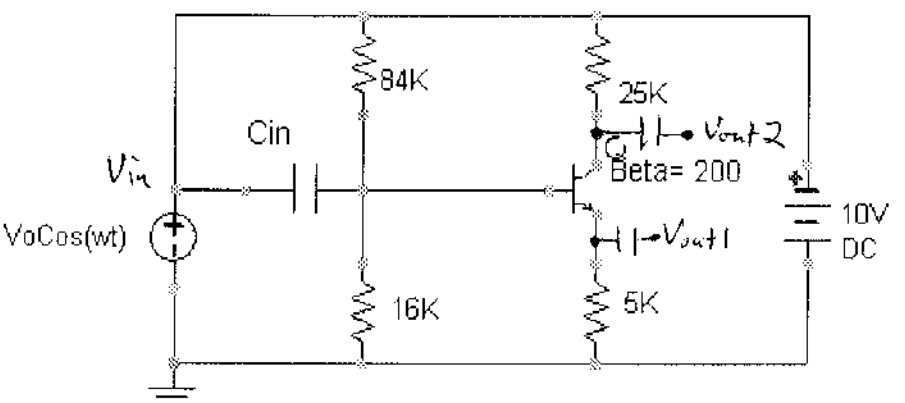
1b.



(see equations on page 5.)

2. For the circuit below in which the transistor is an npn transistor with beta=200
answer the following questions:

a. What is the dc base voltage Vbase?
b. What is the quiescent collector current?
c. What is the intrinsic emitter resistance r_e?
d. What are the effective small signal gains v_{out1}/v_{in} and v_{out2}/v_{in}?
e. For what amplitude of v_{in} will this circuit cease to function as a transistor amplifier? (If v_{in}=Vo.cos(wt),what value of Vo will cause trouble?)



3. For the following circuit, in which the n-channel FET has I_{dss}=6.25ma. and V_t=-2.5V,

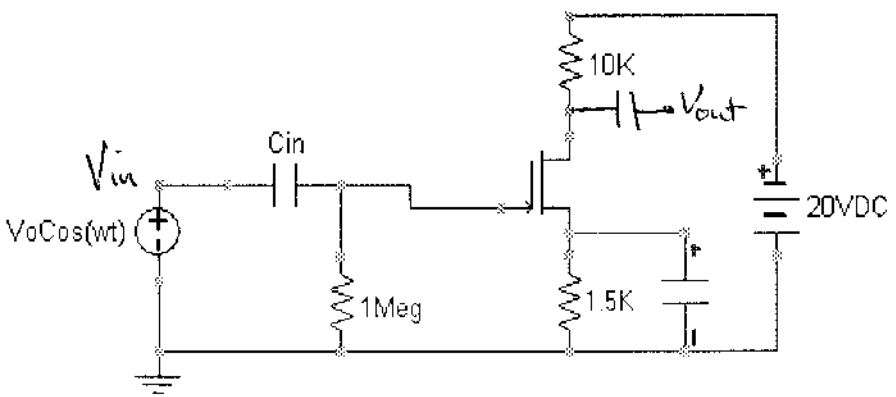
a. Calculate the quiescent current I_d and the quiescent operating voltage V_d.

b. Calculate g_m, the forward transconductance.

c. Assuming C_{bypass} effectively bypasses Rs, what is the small signal gain v_{out}/v_{in} ?

d. What values of C_{bypass} would give a lower 3db cutoff frequency of 100Hz.?

e. What is the effective input impedance seen by the source V_{in}? Assume C_{in} is large enough to ignore.



Some potentially useful equations for the preceding problems:

$$I_c = I_s[\exp(\frac{eV}{kT}) - 1]$$

$$\frac{v_{be}}{i_c} = \frac{25\Omega}{I_c(ma)}$$

$$I_{diode} = I_s[\exp(\frac{eV}{\eta kT}) - 1]$$

$$I_{drain} = k(V_{gs} - V_t)^2$$

$$g_m = 2\sqrt{kI_d}$$

Assume op amp supply pins are connected to +/-10V.

4. Draw op amp circuits using ideal op amps (obeying the 2 golden rules) which will do the following:

a. Give a small signal gain of -10 with an input impedance of approximately 10k ohms.

b. Give a small signal gain of +10 with an input impedance of approx. 100k ohms.

c. Give a differential gain $v_{out}/(v_1-v_2)$ of +10.

d. Give an output voltage $V_{out}=-(2*V_{1in}+3*V_{2in})$.

5. Let A,B,C represent bits such that taken together ABC represent the binary numbers from 0-7. Construct a logic circuit that takes ABC as an input and generates a Q=1 if ABC is divisible by 3 and Q=0 if it is not. (Assume 0 is not evenly divisible by 3.)

a. Construct a truth table for the circuit.

b. Draw a Karnaugh map and identify parts corresponding to logic elements.

c. Write down a Boolean algebraic expression for Q as a function of A,B and C. Reduce it to as simple a form as you can.

d. Design a circuit using standard 2 input logic gates (AND, OR, NAND, NOR, XOR) to perform the logical selection of output states given the inputs.

e. Show how this task may be performed using a multiplexer. Assume you have a chip which accepts ABC as an input and routes one of 8 data lines D0-D7 to the output Q.

5. Let A,B,C represent bits such that taken together ABC represent the binary numbers from 0-7. Construct a logic circuit that takes ABC as an input and generates a Q=1 if ABC is divisible by 3 and Q=0 if it is not. (Assume 0 is not evenly divisible by 3.)

a. Construct a truth table for the circuit.

b. Draw a Karnaugh map and identify parts corresponding to logic elements.

c. Write down a Boolean algebraic expression for Q as a function of A,B and C. Reduce it to as simple a form as you can.

d. Design a circuit using standard 2 input logic gates (AND, OR, NAND, NOR, XOR) to perform the logical selection of output states given the inputs.

e. Show how this task may be performed using a multiplexer. Assume you have a chip which accepts ABC as an input and routes one of 8 data lines D0-D7 to the output Q.

6. Given the transition table for a clocked JK flipflop

J	K	Clock	Q	Q*
0	0	↑	Q_{n-1}	Q^*_{n-1}
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	Q^*_{n-1}	Q_{n-1}

a. Show how using a single inverter you can make a JK flipflop act like a D flipflop. Write the transition table for a D flipflop.
b. Show how you can wire a JK flipflop to act like a "divide by 2" circuit which has as its output a signal 1/2 the frequency of an input clock.
c. given the following circuit:
1. Make a table showing the state of each output and input after each clock pulse. Continue until you see a repeating pattern.
2. Plot the clock, Q1 and Q2 for 10 clock cycles. Assume at the start Q1=Q2=0.
3. How many cycles pass before the pattern repeats?.